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# Chapter 1

## Introduction

This document describes the verification environment for the AXI master dut..

### 1.1 Key features

1. AXI vip can be configured as master/slave

2. All types of AXI transactions are generated

3. AXI slave VIP throws error if any AXI protocol violation detected .

# Chapter 2

## Architecture

### 2.1 Testbench Architectureimage

AXI master dut receives the packets stores from the fifo and sent it to the AXI slave vip. The packet flow is explained below,

* AXI slave vip sends response back to AXI master DUT .
* Read fifo stores the rdata/rdrsp/bresp received by the AXI master DUT.
* Scoreboard compares the packet received by the AXI slave vip and the expected packet sent by FIFO bfm. Write fifo is used to store the axi packets
* Decoder sends the fifo data to the AXI master DUT.
* AXI master DUT transmits the packets on the master interface to the AXI slave vip.

# 

# Chapter 3

## Implementation

### 3.1 FIFO BFM

Below is the path for the FIFO BFM document:

[FIFO BFM doc](https://mirafra2-my.sharepoint.com/:w:/g/personal/deepakrathod_mirafra2_onmicrosoft_com/EbCZuzzEcmtJvJ8C9Bw2jdABJafjT5QNCkowhhWJ8nA8Dw)

# Chapter 4

## Directory Structure

### 4.1.Package Content

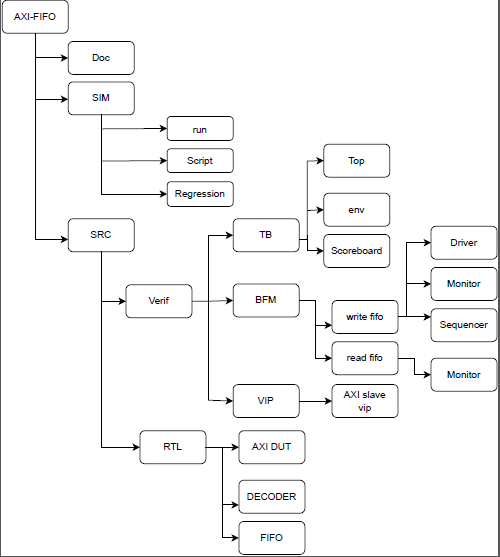


Fig : Directory Structure

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# Chapter 5

**Coverage**

### 5.1 Template of Coverage Plan

Template for Coverage plan is done in an excel sheet and refer to link below:

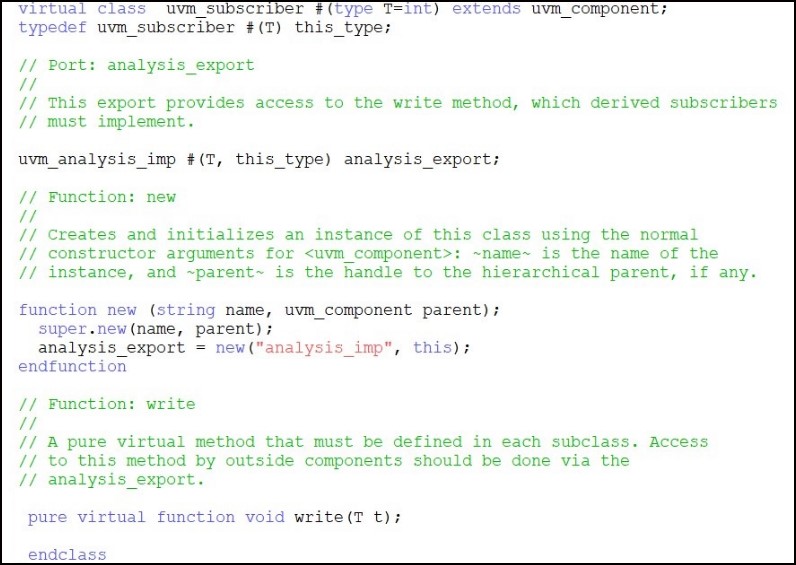
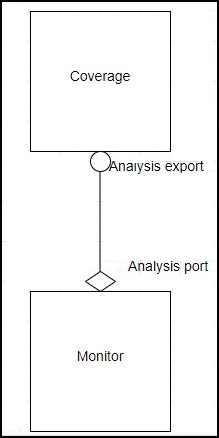
[coverage plan](https://mirafra2-my.sharepoint.com/:x:/g/personal/miteshkhadgi_mirafra2_onmicrosoft_com/EcBZZwuJvJdOtUkUCvtTdYIBzNkKD6hodP8GFzmb4GQa1w)

### 5.2 Functional Coverage

* Functional coverage is the coverage data generated from the user defined functional coverage model and assertions usually written in System Verilog  During simulation, the simulator generates functional coverage based on the stimulus. Looking at the functional coverage data, one can identify the portions of the DUT [Features] verified. Also, it helps us to target the DUT features that are unverified.
* The reason for switching to the functional coverage is that we can create the bins manually as per our requirement while in the code coverage it is generated by the system by itself.

### 5.3 Uvm\_Subscriber

* This class provides an analysis export for receiving transactions from a connected analysis export. Making such a connection "subscribes" this component to any transactions emitted by the connected analysis port. Subtypes of this class must define the write method to process the incoming transactions. This class is particularly useful when designing a coverage collector that attaches to a monitor.



**Fig 7.1.** Uvm\_subscriber

**Fig 7.2.** Monitor and coverage connection

#### 5.3.1 Analysis export

This export provides access to the write method, which derived subscribers must implement.

#### 5.3.2 Write function

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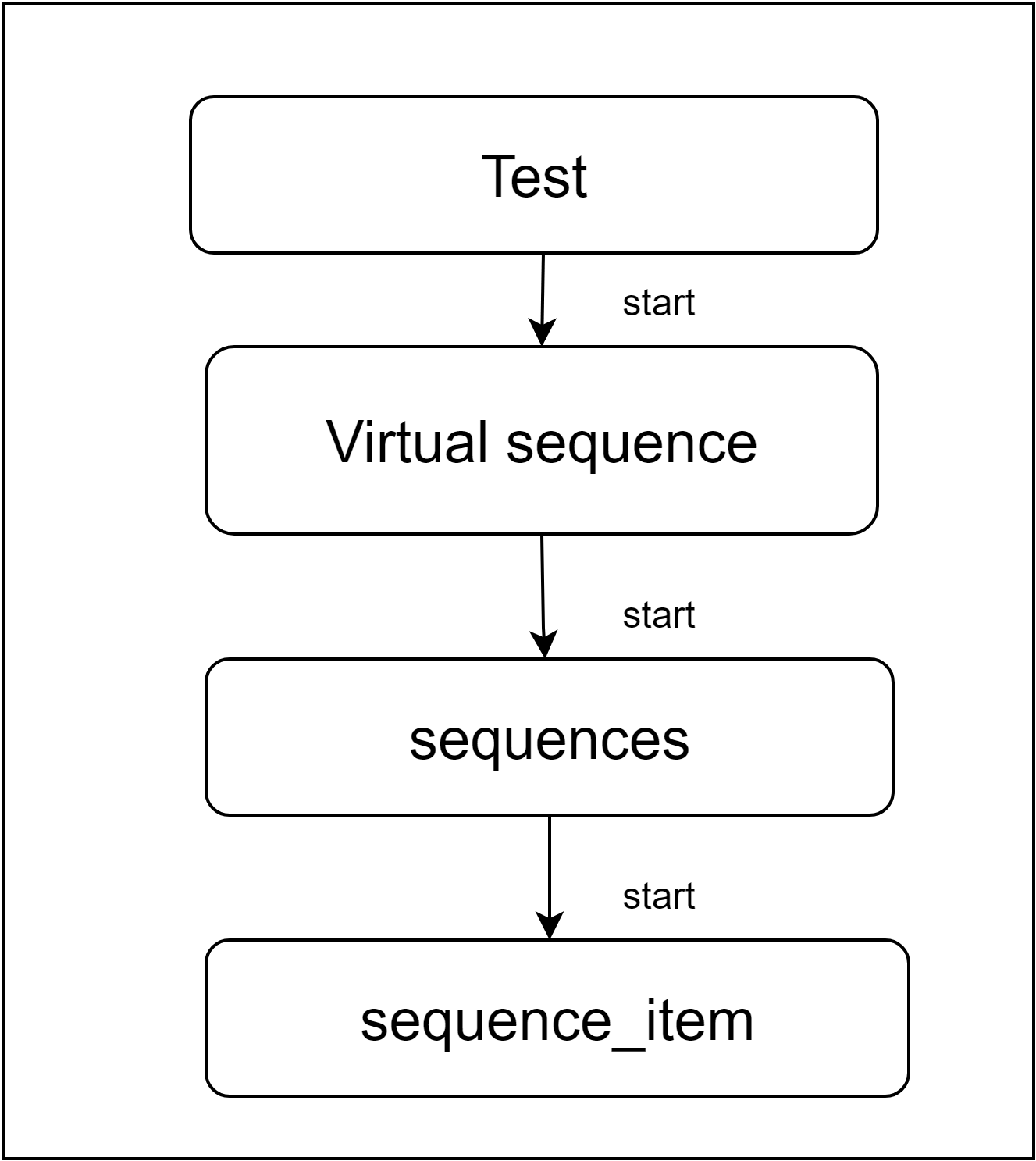
# 

# Chapter 6

## Test Cases

### 6.1 Test Flow

In the test, there is virtual sequence and in virtual sequence, sequences are there, sequence\_item get startedin sequences, sequences will start in virtual sequence and virtual sequence will start in Test.

[](https://app.diagrams.net/?page-id=dnmm31B8M5x43_O-oxbx&scale=auto#G14efqYN0hjCcjijkMFQeD24eAYpKeaZi7)

**Fig 8.1** Test flow

### 6.2 Test Cases

Below is the path for the test case document.

[Testcase doc](https://mirafra2-my.sharepoint.com/:x:/g/personal/zameeraskari_mirafra2_onmicrosoft_com/EdNm9S_PcqVBuMZgMf-RL8wB8a2q8OLagFklreb9jTD6sA)

### 

# Chapter 7

## References

Add the reference document link related to these project